

# AI is outgrowing its hardware; an ASU researcher is developing adaptable chips to meet the challenge

By Kelly deVos, ASU News  
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The old promise of [Moore's Law](#) is simple: Every two years, the future will arrive in the form of faster microchips. For decades, the semiconductor industry delivered that progress. But that era [is fading](#). Today, performance gains are harder to achieve, energy demands are surging, and the idea of a single chip doing everything well is starting to break down.

That is the world [Aman Arora](#) is working in and pushing forward.

Arora is an assistant professor of computer science and engineering in the [School of Computing and Augmented Intelligence](#), part of the [Ira A. Fulton Schools of Engineering](#) at Arizona State University. His research in reconfigurable computing sees the next wave of artificial intelligence, or AI, acceleration not in costly, hotter general-purpose processors, but in hardware that can be targeted to the task at hand.

Arora's tool of choice is the field-programmable gate array, or FPGA, chip, which can be reshaped after it leaves the factory.

"Think of an FPGA as a giant breadboard, an electronics platform where you can wire components together, shrunk down into a tiny chip," Arora says. "You can connect different components however you want, and it becomes whatever kind of circuit you need."

## The accidental engine of AI

The chips that power AI today weren't built for AI at all. They were created for video games.

Graphics processing units, or GPUs, were designed to render online worlds, delivering convincing displays of lighting, shadows and textures. With some adaptation, GPUs quickly became the engine behind modern AI, powering everything from image recognition to large language models.

But they were never designed for what came next.

GPUs are built to handle massive batches of work at once. They excel at training AI models in sprawling data centers, where performance is measured in how much can be processed over time.

But outside the data center, the problem changes. Increasingly, AI is expected to respond instantly — to answer a question, detect a medical anomaly, guide a vehicle or interpret a signal in real time. That stage, known as inference, often prioritizes speed over scale: one request, one answer, as fast as possible.

That is where the cracks start to show.

## **The shape-shifting chip**

Even the most advanced GPUs still rely on the same basic rhythm as traditional processors: fetch instructions, decode them and execute them. They also must constantly move data back and forth through memory.

That overhead adds up. And in a world where AI is moving into phones, sensors and edge devices Edge devices are computing hardware — such as routers or cameras — that reside at the periphery of a network near the data source., it is often too much.

“With an FPGA, there is no instruction decode, no instruction fetch happening,” Arora says. “So no overhead.”

Instead of following instructions step by step, the chip is configured to perform the task directly. Most processors leave the factory with their internal wiring fixed in place, and designing a new chip for every task would be far too slow and expensive.

An FPGA is different. Its internal connections can be reprogrammed after it's fabricated. Load a new configuration, and the chip reshapes itself into a circuit built for that specific job.

Arora is using that flexibility in two ways.

In one direction, his lab is using FPGAs to make AI systems more efficient in the real world. In medical applications, his team is developing systems for glucose monitoring that can run continuously with minimal energy use. In quantum computing, they are building hardware to interpret extremely delicate signals, using machine learning to determine whether a quantum system is reading as a zero or a one. Without that step, the results can't be trusted.

In the other direction, Arora is using AI to improve the chips themselves. Designing an FPGA means choosing from millions of possible ways to configure the chip. His research group is using machine learning to narrow those choices, helping engineers find better designs faster.

## Built to adapt

The result is a shift toward hardware that is not just specialized, but adaptable.

Already in use by [companies like Microsoft](#), FPGAs can be reconfigured as needs change, without being replaced entirely. That makes them especially valuable in places where hardware cannot be easily updated and systems need to adapt to changing demands. The chips are widely used in defense systems and space missions, where high performance is critical and replacing hardware isn't a simple option.

It also changes the economics and environmental cost of computing. Instead of discarding hardware every few years, the same chip can be repeatedly repurposed, reducing both energy use and the need for new manufacturing. And as AI infrastructure scales, cutting wasted computation is becoming just as important as improving performance.

“Some technology companies are buying nuclear power plants to sustain the growth in AI,” he says. “FPGAs are a much more energy-efficient alternative.”

For Arora, the goal is to rethink how technology works together. The future of AI, he argues, will come from designing hardware and software side by side with systems built for specific tasks, but flexible enough to evolve. It is a shift away from the idea of a single, ever-faster machine and toward a tool kit of systems.

In that world, the most powerful computer may not be the one that can do everything. It may be the one that can adapt in ways that matter.

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*This story originally appeared on [ASU News](#).*

<sup>1</sup> Edge devices are computing hardware — such as routers or cameras — that reside at the periphery of a network near the data source.

## Main image



Aman Arora, an assistant professor of computer science and engineering in the School of Computing and Augmented Intelligence, part of the Ira A. Fulton Schools of Engineering at Arizona State University, inspects a field-programmable gate array, or FPGA, chip in his laboratory. Arora leads several microelectronics research projects exploring how adaptable hardware can make artificial intelligence systems faster, more efficient and better suited for real-world environments. Photo by Erika Gronek

**Text image(s)**



Aman Arora at work with students in his laboratory, mentoring a team focused on building flexible hardware. Photo by Erika Gronek